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1.   A system for providing translation between a
host computer having a first port, the first port
compliant with a first standard, and a hardware device
which is compliant with a second standard, the first

5   standard and the second standard being non-compatible
with each other, the system comprising:
        means for direct memory access translation
between the host computer and the hardware device;
        means for supplying power to the hardware

10   device; and
        means for translating the timing between the
host computer and the hardware device such that the
host   computer   and   the   hardware   device   are
interfaced and the functions of the hardware device

15   are provided to the host computer.
2.   A system as defined in claim 1 wherein the
first standard is a PCMCIA standard and wherein the
second standard is an ISA standard.
3.   A system as defined in claim 1 wherein the

20   first standard is a PCMCIA standard and wherein the
second standard is a PCI standard.
4.   A system as defined in claim 1 further
comprising means for interrupt translation between the
host computer and the hardware device.

25   5.   A system as defined in claim 1 wherein the
hardware device comprises at least one ISA compliant
add-on printed circuit card.
6.   A system as defined in claim 1 wherein the
hardware device comprises at least one PCI compliant

30   add-on printed circuit card.
7.   A system as defined in claim 1 wherein means
for direct memory access translation comprises:
        a DMA register; and
        a DMA controller.

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36

8. A system as defined in claim 1 wherein the means for supplying power to the hardware device comprises:

      means for supplying +12 volts;

      means for supplying -12 volts;

      means for supplying +5 volts; and

      means for supplying -5 volts;

all at a current required to operate the hardware device.

9. A system as defined in claim 1 wherein the port comprises a PCMCIA socket.

10. A system as defined in claim 1 wherein the means for translating the timing comprises a read/write timing generator.

11. A system for providing translation between a host computer having a first port, the first port compliant with a first standard, and a hardware device which is compliant with a second standard, the first standard and the second standard being non-compatible with each other and the hardware device requiring support for a plurality of interrupts, the system comprising:

      means for interrupt translation between the host computer and the hardware device;

      means for supplying power to the hardware device; and

      means for translating the timing between the host computer and the hardware device such that the host computer and the hardware device are interfaced and the functions of the hardware device are provided to the host computer.

12. A system as defined in claim 11 wherein the first standard is a PCMCIA standard and wherein the second standard is an ISA standard.

13.   A system as defined in claim 11 wherein the first standard is a PCMCIA standard and wherein the second standard is a PCI standard.

14.   A system as defined in claim 11 wherein the means for interrupt translation comprises means for translating multiple interrupts required by the hardware device to a single interrupt.

15.   A system as defined in claim 14 wherein the multiple interrupts comprises at least five interrupts.

16.   A system as defined in claim 11 wherein the hardware device comprises at least one ISA compliant add-on circuit card.

17.   A system as defined in claim 11 wherein the hardware device comprises at least one PCI compliant add-on circuit card.

18.   A system as defined in claim 11 further comprising means for direct memory access translation.

19.   A system as defined in claim 11 wherein the means for supplying power to the hardware device comprises:

      means for supplying +12 volts;

      means for supplying -12 volts;

      means for supplying +5 volts; and

      means for supplying -5 volts;

all at a current required to operate the hardware device.

20.   A system as defined in claim 11 wherein the port comprises a PCMCIA socket.

21.   A system as defined in claim 11 wherein the means for translating the timing comprises a read/write timing generator.

22.   A system for expanding a host computer having a PCMCIA compliant port and allowing the host computer to interface with at least one ISA compliant device, the system comprising:

38

means for making electrical and physical
connection to the PCMCIA compliant port;

means for making electrical connection to the
at least one ISA compliant device;

means for interrupt translation between the
PCMCIA port and the at least one ISA compliant
device;

means for direct memory access translation
between the PCMCIA port and the at least one ISA
compliant device;

means for providing a clock signal to the ISA
compliant device;

means for supplying power to the at least one
ISA compliant device; and

means for translating the timing between the
PCMCIA port and the ISA compliant device such that
the host computer can utilize the functions of the
at least one ISA compliant device.

23. A system as defined in claim 22 wherein the at
least one ISA compliant device comprises an ISA
compliant add-on card and wherein the system further
comprises a serial port, a parallel port, a key board
port, and a mouse port.

24. A system as defined in claim 22 further
comprising means for providing DRAM refresh to the ISA
compliant device.

25. A system as defined in claim 22 wherein the
means for supplying power comprises:

means for supplying +12 volts;

means for supplying -12 volts;

means for supplying +5 volts; and

means for supplying -5 volts;

all at a current required to operate the hardware
device.

39

26. A system as defined in claim 22 wherein the means for providing a clock signal comprises means for providing an 8 MHz clock signal and means for providing a 14.318 MHz clock signal.

5   27. A system as defined in claim 22 further comprising:

       means for translating a buss address latch enable signal between the PCMCIA port and the at least one ISA compliant device;

10   means for translating between a memory read signal and a memory write signal of the PCMCIA port and a system memory read signal and a system memory write signal for the at least one ISA compliant device; and

15   means for translation between the PCMCIA port and an 8 bit ISA compatible add-on card.

       28. A method for providing translation between a host computer having a first port, the first port compliant with a first standard, and a hardware device

20   which is compliant with a second standard, the first standard and the second standard being non-compatible with each other and the hardware device requiring support for a plurality of interrupts, the method comprising the steps of:

25   translating between the interrupts of the host computer and the interrupts of the hardware device;

       supplying power to the hardware device; and

       translating the timing between the host computer and the hardware device such that the host

30   computer and the hardware device are interfaced and the functions of the hardware device are provided to the host computer.

       29. A method for providing translation between a host computer having a first port, the first port

35   compliant with a first standard, and a hardware device

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which is compliant with a second standard, the first standard and the second standard being non-compatible with each other, the method comprising the steps of:

direct memory access translation between the host computer and the hardware device;

supplying power to the hardware device; and

translating the timing between the host computer and the hardware device such that the host computer and the hardware device are interfaced and the functions of the hardware device are provided to the host computer.

30.   A method for expanding a host computer having a PCMCIA compliant port and allowing the host computer to interface with at least one ISA compliant device, the method comprising the steps of:

making electrical and physical connection to the PCMCIA compliant port;

making electrical connection to the at least one ISA compliant device;

translation between the PCMCIA port interrupt and the interrupts of the at least one ISA compliant device;

direct memory access translation between the PCMCIA port and the at least one ISA compliant device;

providing a clock signal to the ISA compliant device;

supplying power to the at least one ISA compliant device; and

translating the timing between the PCMCIA port and the ISA compliant device such that the host computer can utilize the functions of the at least one ISA compliant device.